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Common-mode termination requirements in concurrent dual-band push-pull power amplifiers

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Common-mode termination requirements in concurrent dual-band push-pull power amplifiers

by

Byron Montgomery

A thesis submitted to the graduate faculty
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Major: Electrical Engineering

Program of Study Committee:
Nathan Neihart, Major Professor
Mani Mina
Randall Geiger

Iowa State University

Ames, Iowa

2017

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DEDICATION

I would like to dedicate this thesis to my brother, Philip A. Montgomery. My life's accomplishments have all been to honor your memory, and I complete this degree to carry on your spirit.

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NOMENCLATURE

3GPP	Third Generation Partnership Project
IEEE	Institute of Electrical and Electronics Engineers
LTE	Long Term Evolution
IoT	Internet of Things
HBT	Hetero-junction Bipolar Transistor
DC	Direct Current
ADS	Advanced Design System

ACKNOWLEDGMENTS

First and foremost, I need to thank my major professor Dr. Nathan M. Neihart, for his guidance and support throughout my academic career at Iowa State. Without his influence, I would never have found RF engineering or been able to push myself to become the person I am today. I would like to thank the members of my committee, Dr. Mani Mina, and Dr. Randall Geiger, both of whom taught me during undergrad and I have come to rely on the lessons learned from them both immensely. Finally, I would like to thank all my friends and the faculty of Iowa State for making my time here so memorable.

ABSTRACT

Concurrent dual-band switch-mode power amplifiers require high common-mode impedance at their intermodulation frequencies. Baluns utilizing quarter-wave effects only present perfect open common-mode impedance at their design frequency. Attempting to use a balun in a dual-band push-pull power amplifier without taking the new dual-band requirements for common-mode impedance into account will result in efficiency loss. This thesis gives a complete derivation of the maximum theoretical drain efficiency in a class-D amplifier, and compares it with the dual-band case using an ideal balun at the output. This ideal balun is explored and the mechanics behind this efficiency loss is revealed. A solution is provided showing that the addition of some transmission lines can move impedance to those specific frequencies by rotation of the common-mode impedance without affecting the differential mode match.

CHAPTER I

INTRODUCTION AND MOTIVATION

1.1 Motivation

In just the past decade, since the invention of the iPhone by Apple, smartphones have become completely ubiquitous in everyday life. Children born today are immersed in touch screens from a very young age and will grow up in a world where every electronic they are exposed to is expected to be connected to the internet. All of these connected devices, from smartphones, to the Internet of Things (IoT), to autonomous vehicles, use an extraordinary amount of bandwidth. It is not going to stop there though, since the establishment of the cellular networks the demand for higher bandwidth and faster speeds have been never ending.

Companies like AT&T and Ericsson have been attempting to provide forecasts of mobile traffic for years in order to see how they should build their networks and phones to accommodate

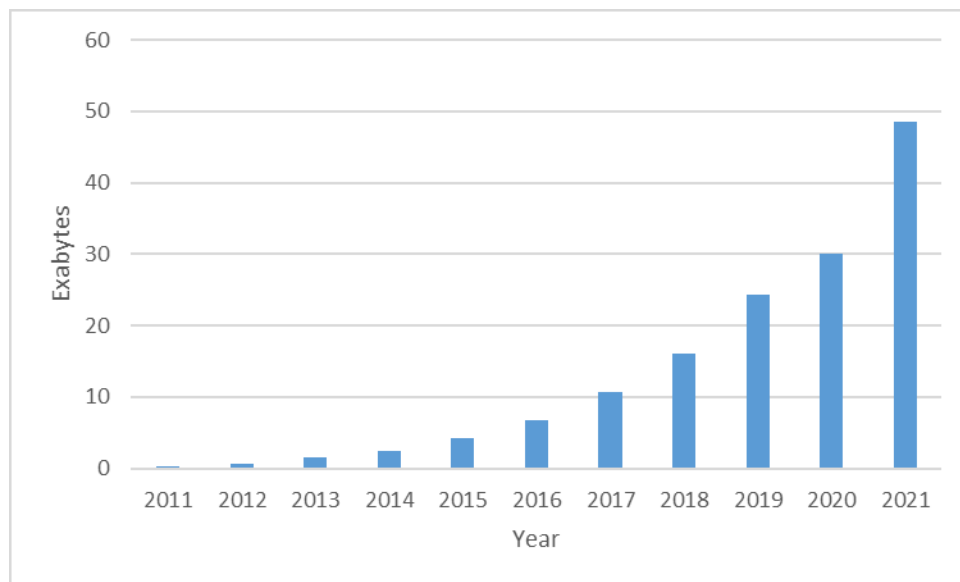


Figure I-1 *Worldwide monthly data forecast*

the public, and what they have found shows an exponential growth in data consumption. By 2021 the global data consumption could reach as high as 50 Exabytes a month [1]. To further exacerbate this issue, other countries populations haven't even begun to come online to the extent North America has. This is not limited to commercial devices either, military applications have seen bandwidth demands increase as well while tactical data becomes increasingly complex and encrypted.

In order to respond to the ever-increasing demands for more bandwidth, the Third Generation Partnership Project (3GPP) has begun releasing new Carrier Aggregation (CA) standards to increase the efficiency of the available spectrum. Carrier Aggregation allows cellular devices to transmit and receive on more than one band simultaneously which increases the bandwidth that each device can utilize, thus increasing the maximum bitrate that the device can support. There are already hundreds of different CA bands defined even though most have yet to be fully utilized in current phone designs [2, 3] Currently when transmitting on a single band the maximum channel bandwidth is 20MHz, the benefits of carrier aggregation are plain to see.

Figure I-2 shows a CA band that is already released, specifically band 1A-3A-5A. There are some devices currently on the market that are capable of utilizing this CA band, and it allows

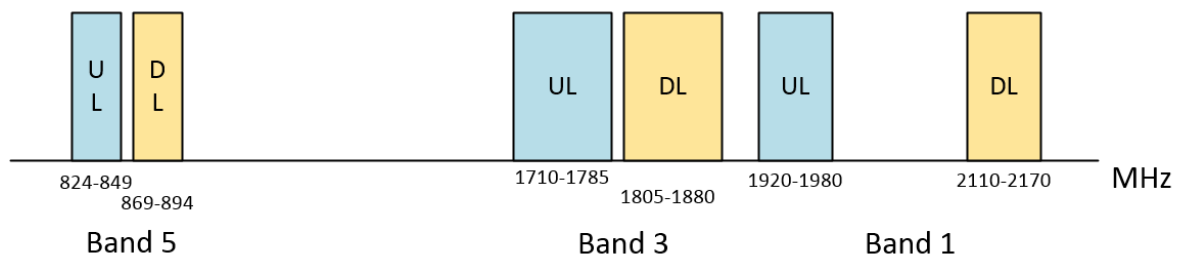


Figure I-2 Carrier aggregation band 1A-3A-5A

for a maximum aggregated bandwidth of 50MHz. Now the task has fallen to the engineers and designers that will build these phones and base stations to support simultaneous transmission of two or more carriers. Current front-end modules may have several separate radio frequency (RF) paths, each with their own switches and amplifiers, which significantly increases the complexity as well as the area required. A good example of a cutting edge front-end module is the SkyOne3.0 which is a family of products that can support bands 1, 2, 3, 4, 5, 8, 12, 13, 17, and 28 [3]. The block diagram for a SkyOne 3.0 front-end is shown in figure 3. A cursory glance shows 17 matching networks, 6 amplifiers, 7 multiple throw switches, and 8 diplexers/filters, all of these support their own frequencies. While many of the frequency ranges overlap for some consolidation, there are still 13 individual RF paths all on the same front end module. Currently for this device only one band transmits at any given time, but when LTE-A is implemented, two or more RF paths will be transmitting simultaneously, each one would need to be further isolated from one another than they already are to prevent instability or crosstalk.

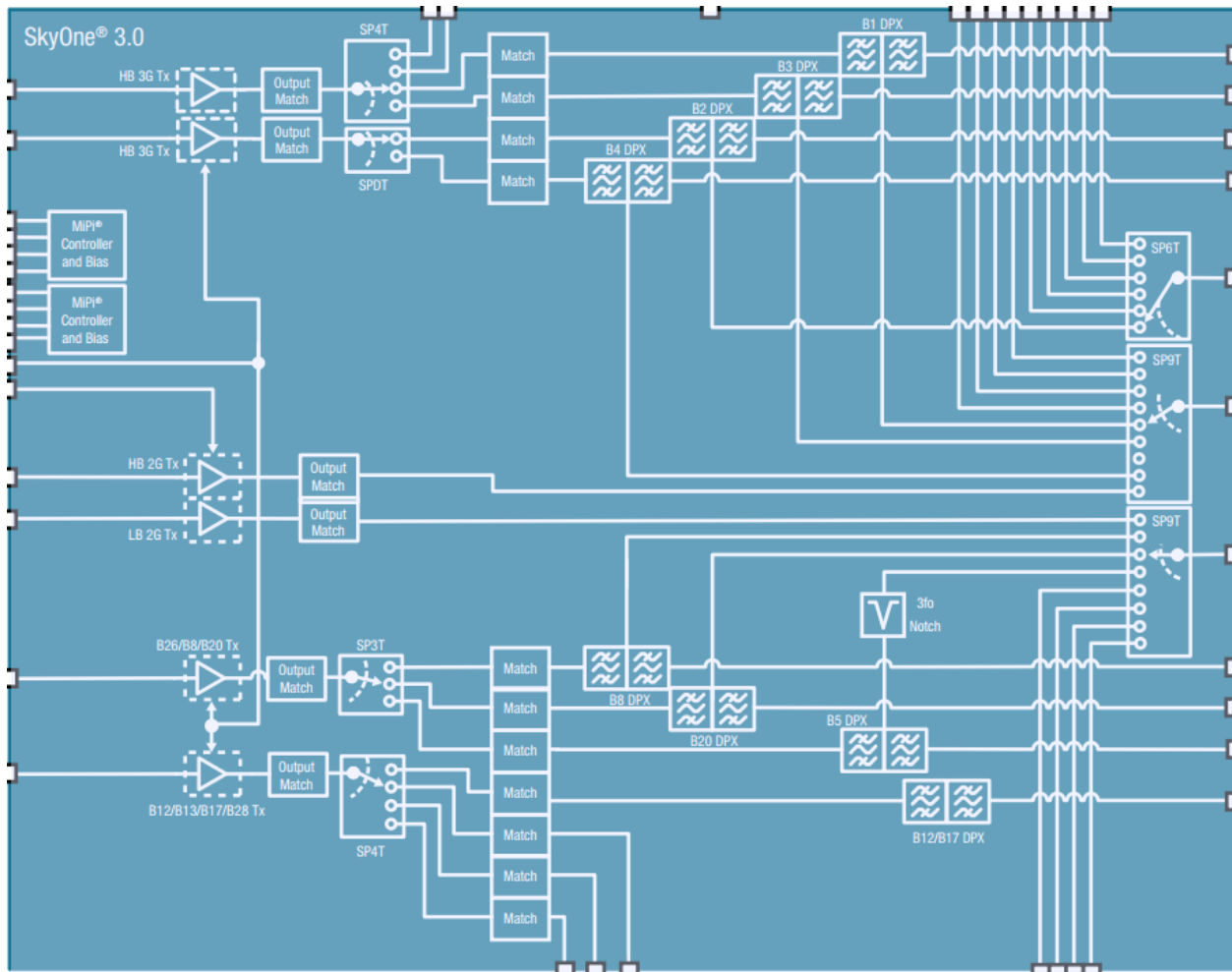


Figure I-3 Block diagram of SkyOne3.0, a front-end module by Skyworks Solutions, Inc.

The front-end module shown in fig. 3 is an attempt to consolidate the support of all these bands onto a single transceiver module. It is clear that even though this is one of the latest designs available the ability to merge any of these devices or paths together would allow for significant space savings which would reduce the cost substantially. To achieve this, engineers have begun pursuing solutions that allow a single amplifier to transmit on multiple frequencies simultaneously [4, 5].

1.2 Thesis Organization

With carrier aggregation on the horizon and designers already supporting tens of bands on each device the need to consolidate and merge has become great. Amplifiers that can transmit multiple carriers simultaneously have begun to be collected under the term “concurrent-band amplifiers” even though their design and construction have yet to be thoroughly researched, especially in the non-linear amplifier classes. Single-band variants of these amplifiers have been built and the problems encountered in their design are well documented [6, 7]. This thesis provides an overview of the different problems that can occur in push-pull amplifiers when engineers attempt to drive it with two or more carriers simultaneously. In applications requiring high output power and high efficiency a push-pull switched-mode amplifier would be an appropriate choice giving an added 3 dB of maximum output power while also reducing noise from even harmonics [8, 9]. The final output from an amplifier can be required to be single-ended, for either an antenna, or other signal processing stages. It is due to this reason that push-pull amplifiers typically require a transformer for differential to single ended conversion. Transformers however, are difficult to realize at RF frequencies. For example, the needed ferrite cores are limited to applications less than 500 MHz and their use in higher frequency transformers cause them to become lossy and bulky. A popular choice is to use capacitively coupled microstrip baluns instead.

Planar baluns utilize the properties of coupled transmission lines and quarter-wave effects to approximate the behavior of a transformer and have three key parameters that designers attempt to maximize in single-carrier design. A well-designed balun has low insertion loss, good amplitude/phase balance, and high common-mode rejection ratio (CMRR) [11]. A significant difference between a transformer and a balun, however, is that a balun does not have a common-

mode port, which is not an issue in single-carrier designs since the coupled lines cannot support common-mode signals at the quarter-wavelength frequency. In fact, the impedance seen by a common-mode excitation is an open-circuit at the design frequency and it is relatively easy to achieve high CMRR over the entire operating range for planar baluns [12, 13].

However, in dual-carrier designs there are two design frequencies, f_1 and f_2 , and the common-mode voltage now becomes a full-wave rectified version of the sum of two sine waves consisting of the IM components of f_1 and f_2 . This changes the common-mode termination requirements. Instead of requiring an open circuit at even harmonics, an open circuit termination is now required at the frequency of the IM components and having high CMRR does not necessarily guarantee that a high impedance is presented to the common-mode signals since common-mode signals can also be rejected by shorting them to ground. Since planar baluns can no longer rely on the periodicity of their structure to suppress the common-mode in dual-carrier class-D PAs, designers must modify their baluns to account for this, or face the efficiency losses associated common-mode power leakage. This is the main phenomena that will be explained in this paper. First it will explore the new requirements in a concurrent-band push-pull Class-D power amplifier with a complete overview of single-band Class-D operation, followed by a dual-band overview contrasting the differences. Secondly, the full ramifications of ignoring these new requirements will be calculated in MATLAB and verified using Keysight's Advanced Design System (ADS). Then, some example dual-band baluns will be designed and it will be shown that even though they have desirable properties at both frequencies their common mode impedance will not be sufficient without changes. Finally, a simple method for alleviating any efficiency loss by modifying the existing balun with those changes designs will be shown.

CHAPTER II

CLASS-D POWER AMPLIFIERS

2.1 Overview

This chapter will provide a complete derivation of the maximum theoretical efficiency for a single-band class-D amplifier and contrast the result with the dual-band case. The class-D amplifier is still relatively uncommon at RF frequencies due to how difficult it has been to realize transistors with the fast switching behavior required. However, with high-speed GaN HEMTs class-D behavior is achievable. In a push-pull configuration, you can design for high output powers while still preserving the 100% maximum theoretical efficiency [7, 8, 9].

2.2 Single-Band Theoretical Drain Efficiency

The principle at work in the class-D amplifier is that each transistor is only conducting when there is no voltage drop from drain to source, thus in the ideal case, no power will be consumed inside the transistors. Before the derivation can begin a few assumptions have to be made clear. For one, it is assumed that the amplifier shown in Fig. II-4. has transistors that behave as ideal switches with zero ON resistance and infinite OFF resistance, secondly, the RF

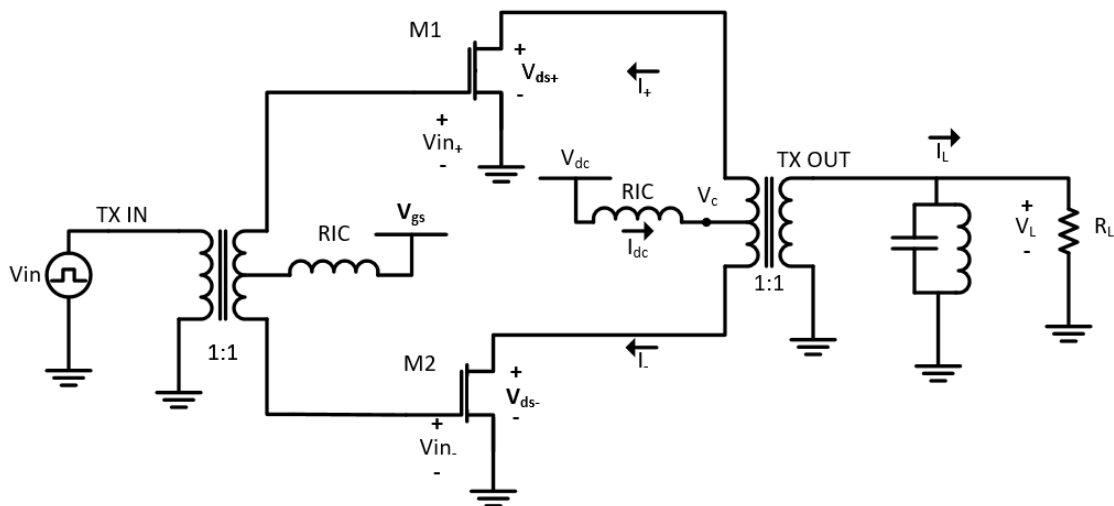


Figure II-4 The schematic of a class-D amplifier

choke inductors have infinite inductance and conduct a constant current, and finally, this derivation will be done on a current-switching architecture. A current-switching architecture means that the transistors will allow their maximum current to flow through them because the voltage at the gate will be high enough to place it in saturation. To calculate the maximum drain efficiency, we will start with the input voltage. V_{in} is defined to be a square wave as:

$$V_{in} = \text{sgn}(\sin(\omega_0 t)) \quad (\text{II-1})$$

The input V_{in} goes through a transformer, or balun, in order to split the input into two equal yet antiphase signals, V_{in+} and V_{in-} . For convenience it will be assumed that both the input and output transformers are ideal with a 1:1 turns ratio so that the differential signals at the gate of the transistors can be expressed as:

$$V_{in+} = \text{sgn}(\sin(\omega_0 t)) \quad (\text{II-2})$$

$$V_{in-} = -\text{sgn}(\sin(\omega_0 t)) \quad (\text{II-3})$$

Since the output transformer is also ideal the output current will be formed purely by the LC tank, which for these purposes is comprised of an ideal inductor and capacitor with infinite Q, making the load current I_L and load voltage V_L pure sinusoids. I_L and V_L can be expressed as:

$$I_L = \frac{4}{\pi} I_{DC}(\sin(\omega_0 t)) \quad (\text{II-4})$$

$$V_L = I_L R_L = \frac{4}{\pi} I_{DC}(\sin(\omega_0 t)) R_L \quad (\text{II-5})$$

where I_{DC} is the dc current coming from the supply V_{DC} , later these values will be calculated as well. From this point, since the single-ended voltage from the output of the ideal transformer is known therefore the drain voltages can be expressed as:

$$V_{ds+} = \begin{cases} 2V_L \sin(\omega_0 t) & \text{for } 0 \leq t \leq T/2 \\ 0 & \text{for } T/2 < t < T \end{cases} \quad (\text{II-6})$$

$$V_{ds-} = \begin{cases} 0 & \text{for } 0 \leq t \leq T/2 \\ 2V_L \sin(\omega_0 t) & \text{for } T/2 < t < T \end{cases} \quad (\text{II-7})$$

Because it's assumed that the transistors behave as ideal switches the drain currents will simply be square waves both of which have the same fundamental frequency. The drain currents can be expressed in the form of two pulse trains

$$I_+ = \begin{cases} I_{dc} & \text{for } 0 \leq t \leq T/2 \\ 0 & \text{for } T/2 < t < T \end{cases} \quad (\text{II-8})$$

$$I_- = \begin{cases} 0 & \text{for } 0 \leq t \leq T/2 \\ I_{dc} & \text{for } T/2 < t < T \end{cases} \quad (\text{II-9})$$

When plotted, the drain voltages and currents never overlap and are antiphase.

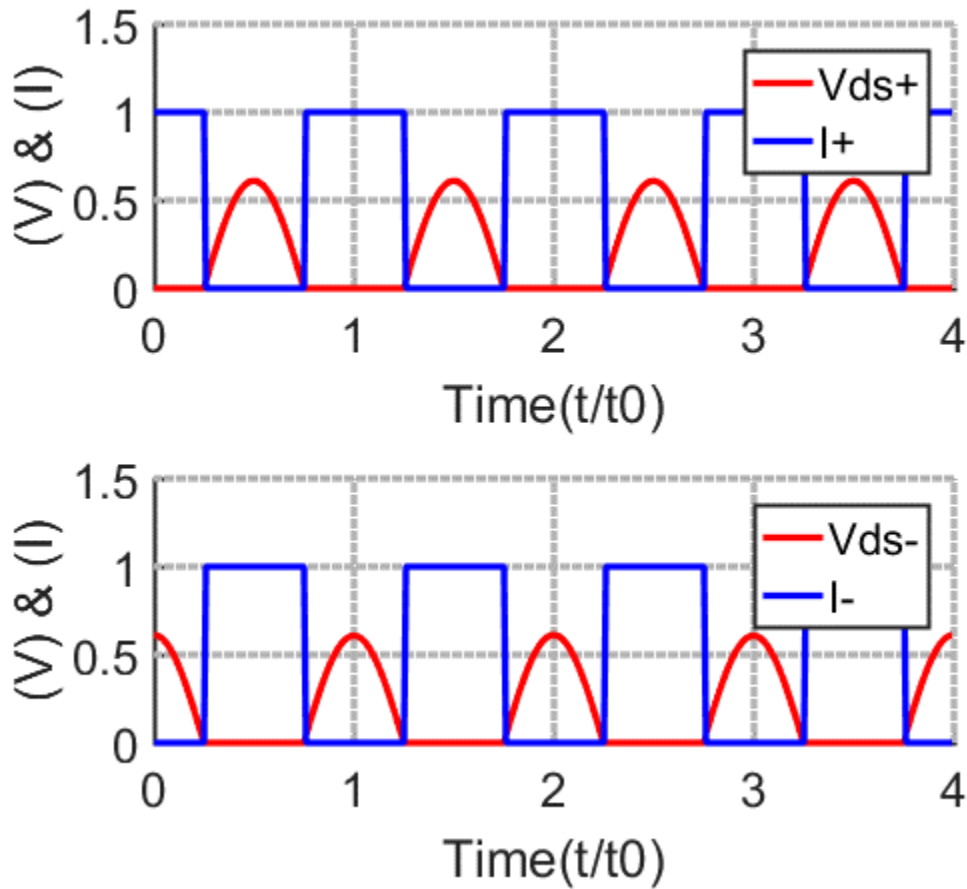


Figure II-5 Single-band voltage and current at the drains in a class-D amplifier

Also, since the current in both drains is coming from the same node it's known that:

$$I_{dc} = I_+ + I_- \quad (II-10)$$

$$V_C = |V_{ds+} + V_{ds-}| \quad (II-11)$$

Continuing on, the drain currents and voltages are shown in Fig II-5. The last step in determining the maximum efficiency is calculating values for I_{DC} and V_{DC} . The DC supply voltage, V_{DC} can be calculated by finding the average value of the center tap voltage V_C and using equations (II-7) and (II-8). Since V_C is equal to half of the sum of the two sine waves V_{ds+} and V_{ds-} it's average can be calculated here:

$$V_C = \frac{1}{2\pi} * \int_0^{2\pi} \left[\frac{V_{ds+}}{2} + \frac{V_{ds-}}{2} \right] dwt = \frac{8}{\pi^2} * I_{dc} R_L \quad (II-12)$$

From here I_{DC} can be calculated as:

$$I_{dc} = \frac{\pi^2}{8} * \frac{V_{dc}}{R_L} \quad (II-13)$$

And finally the efficiency becomes:

$$\eta = \frac{\frac{1}{2} I_L^2 R_L}{V_{dc} I_{dc}} = 100\% \quad (II-14)$$

To make this a complete derivation the output power P at the fundamental frequency seen by the load can be solved for using equations (II-4) (II-5) (II-13)

$$P = \frac{8}{\pi^2} I_L^2 R_L \quad (II-15)$$

This result here has been well established for quite some time, and although it's ramifications are important [15]; this paper is more concerned with how the efficiency changes in a concurrent-band architecture. To demonstrate this, the common mode voltage seen at the center tap of the output transformer needs to be examined closely. A little rearranging of terms

will show that the voltage V_C is a full wave rectified version of the differential voltage V_L . The Fourier series representation needs to be calculated in order to see the difference between the dual and single band case. There are a couple different ways to calculate this Fourier series, the most common involving combining the Fourier series of two half-rectified sine waves, each offset by $\frac{\pi}{2}$. Either way the result will be as follows, for those seeking further clarification the Wolfram Mathematica file has been included in Appendix 1.

$$|V_L \sin(\omega_0 t)| = \frac{2V_L}{\pi} - \frac{4V_L}{\pi} \sum_{n=2,4,\dots}^{\infty} \frac{\cos(n\omega_0 t)}{n^2-1}. \quad (\text{II-14})$$

The spectrum of this common mode voltage is plotted in Fig. II-6, it's comprised of even harmonics and an average value (not shown) which was also calculated in (II-12). However, as was stated earlier, higher frequency designs cannot use magnetic transformers and designers often turn to planar transmission line baluns. There's nothing wrong with this strategy for the single band case since planar baluns typically rely on quarter-wavelength effects which will show a perfect open or short at harmonics.

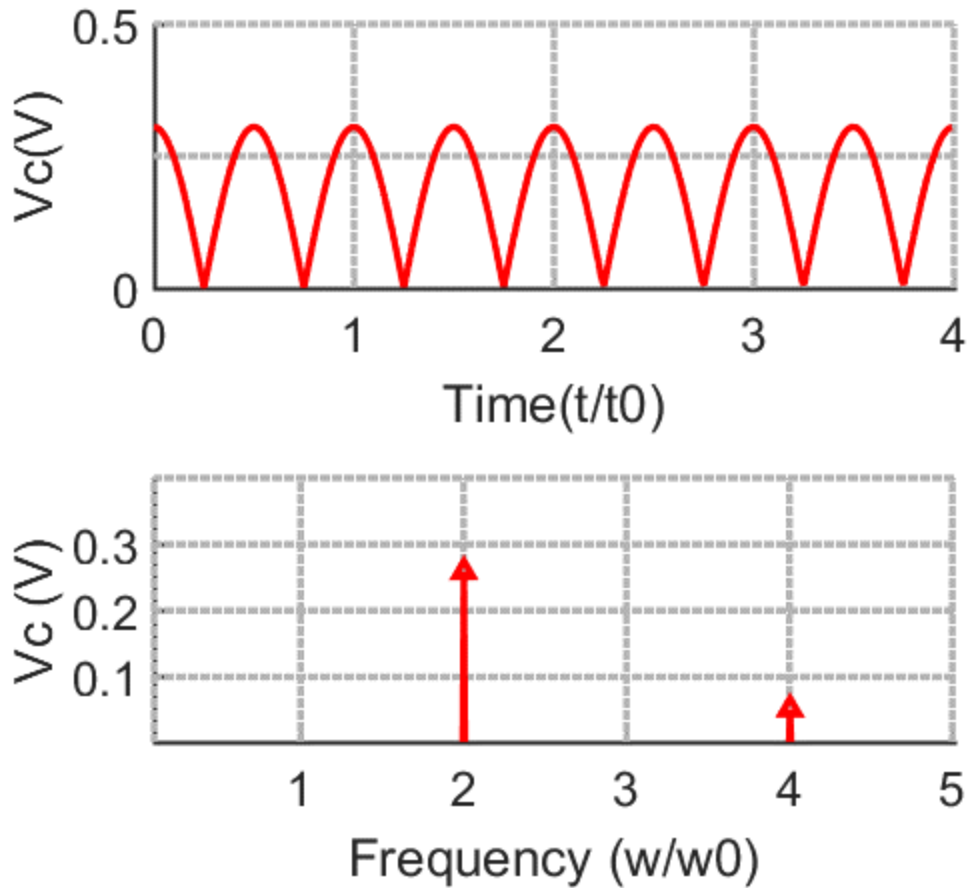


Figure II-6 Common voltage seen at the transformers center tap in a push pull class-D amplifier.

However, many of the assumptions that can be made in single-band amplifiers simply do not apply when designing for dual-band ones. Specifically, when it comes to how the common-mode is terminated, extra care must be given since there is no longer only even harmonics present in the common-mode, but even intermodulation components, which is shown in the next chapter.

CHAPTER III

DUAL-BAND CLASS-D POWER AMPLIFIERS

3.1 Overview

As has been stated earlier the ability to consolidate multiple carriers onto a single RF path would be highly desirable in today's over-crowded front-end module designs. However, dual-carrier PA's have yet to be widely researched, there have been some papers published that go over their design but they generally only cover single-ended architectures [8, 18], Or they might only cover concurrent band impedance matching [17, 28], It's important to note however that management of the intermodulation components for increased efficiency has been done but only in single-band [9]. Although these researchers are using them for waveform shaping of the output to improve efficiency. From here we're going to repeat the same exercise that was done in chapter II but with a key difference of two fundamental frequencies being amplified at the same time. Comparisons will be drawn and conclusions made about how these two similar setups differ in important ways.

Using the same schematic for a class-D amplifier as shown in Fig. II-4 with a few exceptions, it's assumed that the output resonator now resonates at two frequencies, ω_{lo} and ω_{hi} . The input V_{in} is now defined as the sum of two sinusoids:

$$V_{in} = \mathbf{sgn}(\mathbf{sin}(\omega_{lo}t) + \mathbf{sin}(\omega_{hi}t)) \quad (\text{III-16})$$

Knowing that the transistors are still ideal switches the drain current become:

$$I_{+} = \mathbf{sgn}(\mathbf{sin}(\omega_{lo}t) + \mathbf{sin}(\omega_{hi}t)) \quad (\text{III-17})$$

$$I_{-} = -\mathbf{sgn}(\mathbf{sin}(\omega_{lo}t) + \mathbf{sin}(\omega_{hi}t)) \quad (\text{III-18})$$

Again, since the transistors are working as ideal switches, whenever the input voltage is greater than zero the maximum amount of current will begin flowing from drain to source. This

will change the drain currents into a complex sum of pulse trains. Furthermore, we assume that the ideal LC tank is now a resonator at two frequencies, meaning the differential voltage must be equal to:

$$V_L = I_L * R_L = \frac{4}{\pi} * I_{dc}(\sin(\omega_{lo}t) + \sin(\omega_{hi}t)) * R_L \quad (\text{III-19})$$

The single-ended voltage at the load allows us to calculate the differential voltages present at each drain by using the ideal balun equations.

$$V_{diff} = V_+ - V_- \quad (\text{III-20})$$

$$V_{com} = \frac{V_+ + V_-}{2} \quad (\text{III-21})$$

$$I_{diff} = -1 * \frac{I_+ - I_-}{2} \quad (\text{III-22})$$

$$I_{com} = I_+ - I_- \quad (\text{III-23})$$

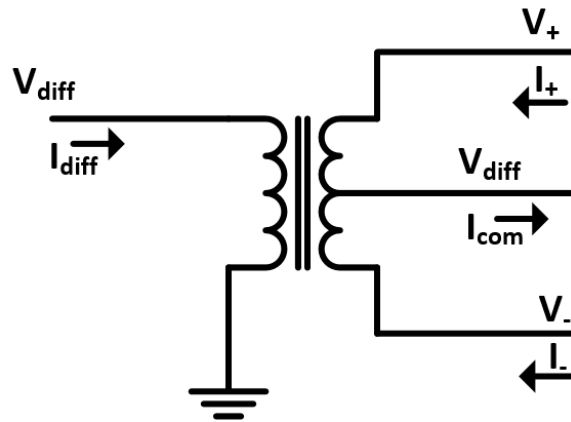


Figure III-7 Example schematic for an ideal transformer/balun.

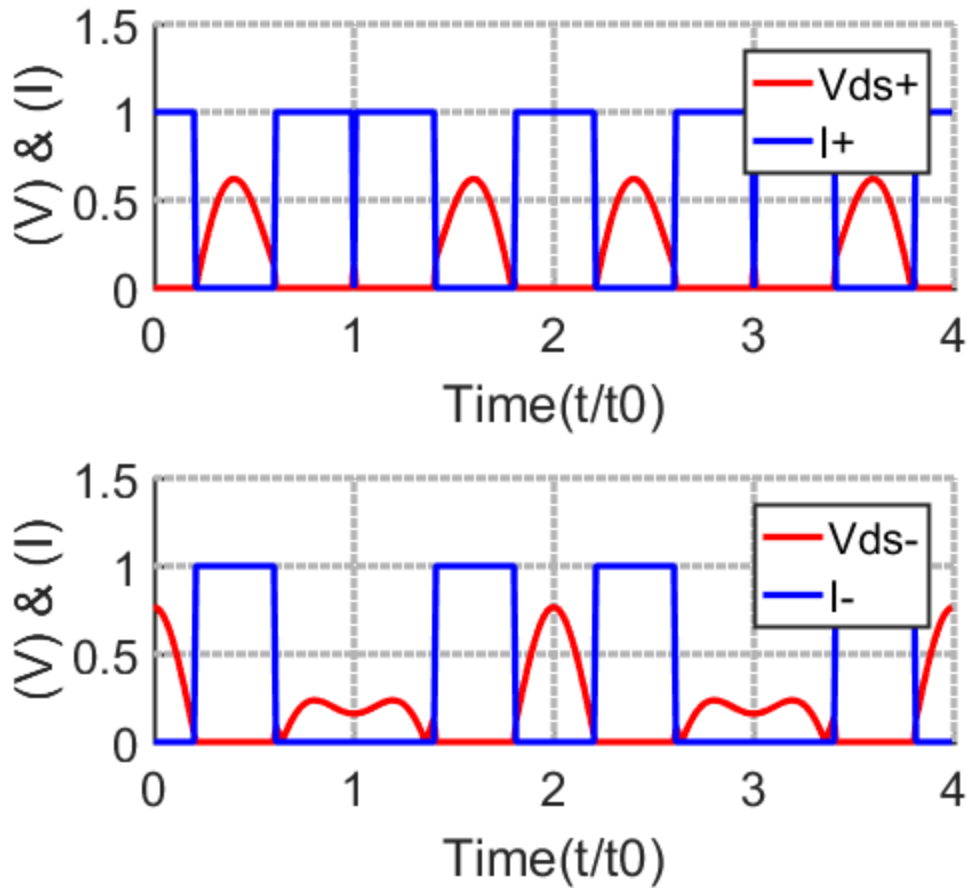


Figure III-8 Drain current and voltage seen at the transformers center tap in a dual-band push pull Class-D amplifier

The drain currents and voltages are plotted in Fig. III-8. It's known that at the common mode output the voltage will be half the magnitude of the two differential voltages. Adding them together will result in a rectified sum of two sinusoids, and while the common mode voltage in the single band case is calculable through some Fourier series manipulation tricks, the dual-band case is significantly more complex but can be done numerically the Mathematica code for which is included in Appendix B.

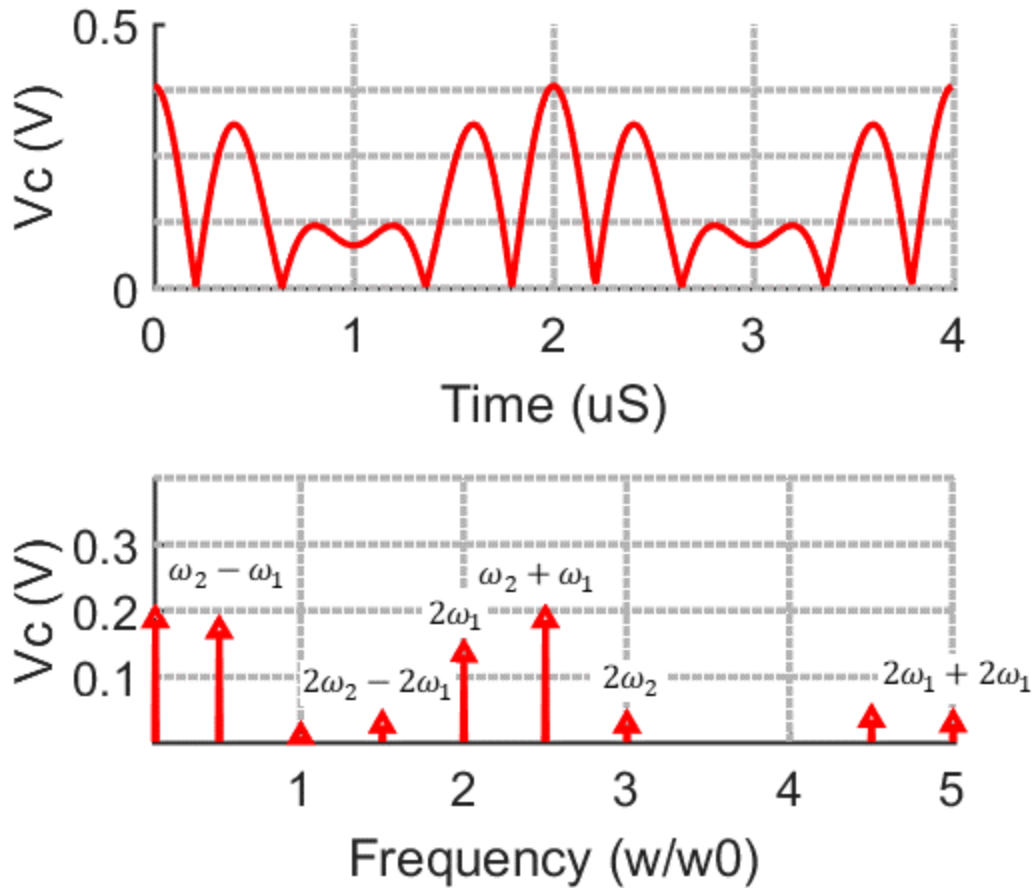


Figure III-9 Common-Mode voltage seen at the transformers center tap in a push pull dual-band Class-D amplifier

The first thing to notice from the Fourier series in Fig. III-9. is that it has many more components than the single band case. It consists of a DC offset, several even harmonics, and most noticeably, a number of even intermodulation components. These intermodulation components become a problem when selecting a differential to single-ended converter. It is important to note that the presence of these intermodulation components is not due to the non-linearity of the transistors since in this model we are assuming an ideal switch, which is not to say that in a non-linear device they would not also be a contributing factor. These

intermodulation components are generated by the intrinsic nature of the balun or transformer, and will be present in any device that has a similar non-overlapping waveform such as Classes E and F. The intermodulation components generated by the devices non-linearity would be present in the linear amplifier classes such as classes A, AB, B, and C, those however are not addressed by this paper but would make interesting study.

3.2 MATLAB Verification

The presence of these additional frequency components dramatically complicates the common-mode termination requirements when compared to the single band case. The problem is now if a dual-band push-pull power amplifier was used with a balun that was not specifically designed to present open common-mode impedance at its intermodulation frequencies then power will begin to leak through the transistors as the voltages and currents at the Drains will begin to distort and overlap. In the ideal case, all the common-mode voltage components are terminated in a perfect open, which would result in a Drain efficiency of 100%. There are two potential problems with achieving a result close to ideal, the first being that it is impractical to terminate all the frequency components in the common-mode voltage. There are simply too many to be able to design a balun that accommodates all possible frequency combinations while already providing a matched differential impedance. The second being it is already difficult to achieve an open-circuit common mode termination. To combat this a designer would go for a common-sense approach, which of these frequency components matter the most and if a perfect-open isn't feasible then how high does the impedance need to be? It's very rare to see an issue in RF design crop up of from anything beyond the 5th harmonic since harmonics fall off in magnitude as frequency increases, the same is true for intermodulation components [15]. In practical terms, impedance matching for perfect opens and shorts is impossible and 1:1 VSWR

matches do not truly exist. The question a designer will seek to answer is what impedance value is high enough, and which intermodulation components are most important in order to salvage as much efficiency as possible. To answer these questions, the effects of common-mode power leakage were examined through numerical analysis using MATLAB, and verified in ADS for an ideal class-D push-pull power amplifier. A complete copy of the MATLAB script is included in Appendix A.

In a dual-band amplifier, efficiency is defined as:

$$\eta = \frac{P_{\omega_{lo}} + P_{\omega_{hi}}}{P_{dc}} = 100\% \quad (\text{III-24})$$

Where $P_{\omega_{lo}}$ is the RF output power for ω_{lo} and $P_{\omega_{hi}}$ is the RF output power for ω_{hi} . As was stated earlier, taking the Fourier transform of the rectified sum of sinusoids is possible, but the reader will find it greatly simplified to set ω_{hi} equal to $x\omega_{lo}$:

$$F(\omega) = \int_{-\infty}^{\infty} |\sin(\omega_{lo}t) + \sin(\omega_{hi}t)| dt \quad (\text{III-25})$$

Where x is the ratio between the two frequencies. The results of this equation are in the appendix, but for the sake of simplicity, the MATLAB script performs all these calculations numerically taking the frequencies as inputs. First, the script computes the Fourier series coefficients of the common-mode voltage and then proceeds to terminate each component, one at a time, with an impedance normalized to the load resistance. The other frequency components are terminated with an ideal open. Each time it recalculates the Drain voltages and currents and determines the new RF output power for each fundamental.

Table 1 Efficiency loss due to the common-mode power leakage in push-pull class-D PA.

Common-mode Termination	Common-Mode Component $\omega_2 > \omega_1$					
	$\omega_2 + \omega_1$	$2\omega_2 - 2\omega_1$	$2\omega_1$	$\omega_2 - \omega_1$	$2\omega_2$	$2\omega_1 + 2\omega_1$
$R_L/10$	-39%	-11%	-18%	-35%	-17%	-11%
$R_L/5$	-27%	-5.80%	-11%	-24%	-9%	-6%
$R_L/2$	-13%	-2%	-5%	-12%	-4%	-2%
R_L	-7%	-1%	-2%	-7%	-2%	-1%
$2R_L$	-4%	-1%	-2%	-3%	-1%	-1%
$5R_L$	-1%	<-1%	<-1%	-1%	<-1%	<-1%
$10R_L$	-1%	<-1%	<-1%	<-1%	<-1%	<-1%

Table 1 shows the results of the MATLAB script, in terms of the amount of efficiency loss from the ideal case. If we compare this table with Fig. III-9 the frequency components with the higher magnitudes waste the most efficiency. Components with lower magnitude and also higher intermodulation order have a comparatively smaller effect on efficiency,

III-3 ADS Simulation

This result was similarly verified in ADS, using a simplified ideal transistor and equation-based component models. The switch shown in Fig. III-10 is a mathematically rigorous way to implement an ideal transistor in ADS. There are other ways using equation based components, but this way works best for our purposes and does not return any convergence errors. A simple Z11 component that is an open at the two frequencies of interest and a thru for all else can be used for the ideal LC tank. The only other thing needed to perform this verification is ensuring your harmonic balance settings will capture the intermodulation components. The simulation time will be severely extended, but if the maximum mixing order is not set high enough the resulting waveforms will be inaccurate. Shown in Fig. III-11 is a well-balanced approximation of the ideal waveforms seen in ADS. The output here uses a very low r_{ds} of 200 $m\Omega$, a near-zero turn-on threshold, and a near-infinite off resistance. The common mode shown earlier in Fig. III-9 is the same as the one seen in ADS. When you add the two uneven differential voltages

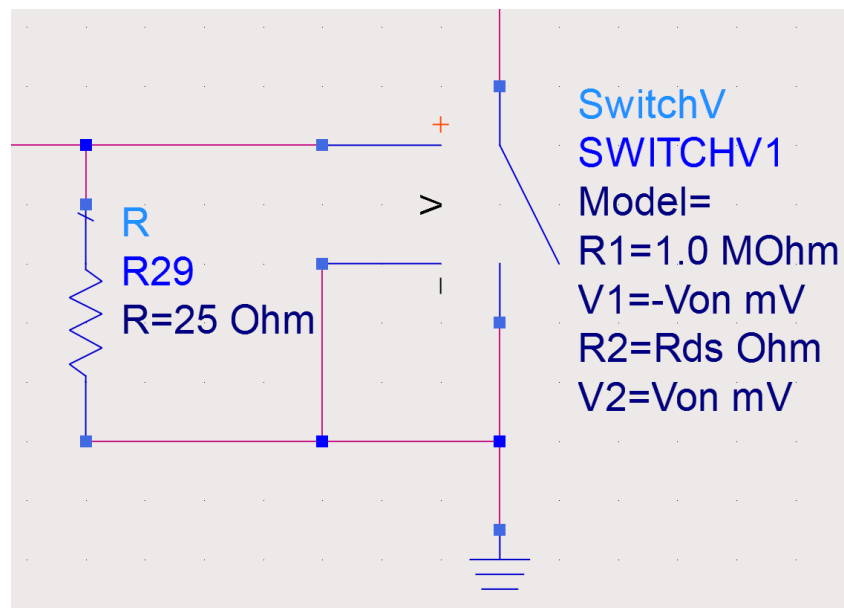


Figure III-10 Ideal transistor used for efficiency loss verification

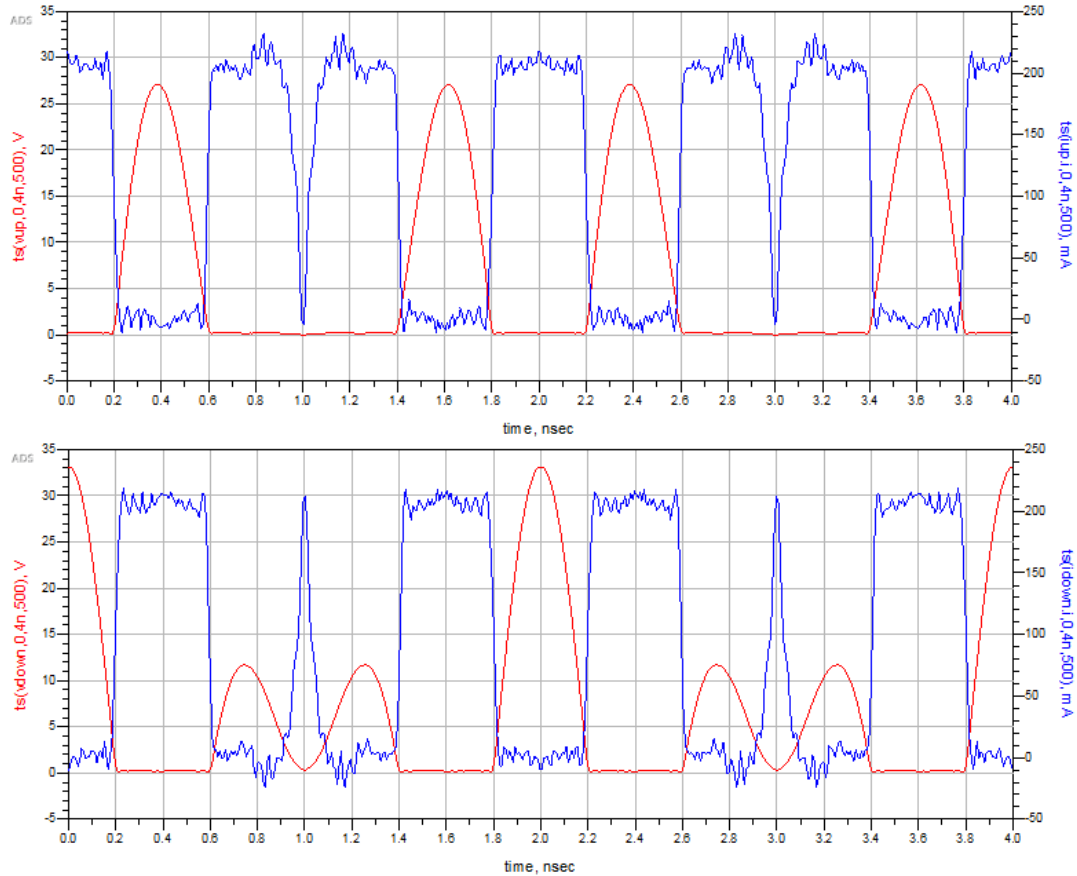


Figure III-11 Resulting waveforms from ADS

together, you get the same rectified sum of two sine waves. This has the same spectral content as before and not presenting those components with a high impedance will directly affect efficiency. Running harmonic balance simulations on our ideal dual-band class-d amplifier with an adequately high simulation order and perfectly matched output transformer with no loss will return the waveforms see in Fig. III-11. These waveforms are very close to what was predicted using MATLAB, and using ADS to calculate the drain efficiency using the same formulas in Chapter II. returns a value of 93.0%. Now that the ideal amplifier has been verified we can modify the output balun/transformer using equation based elements to show any impedance value to any common mode frequency desired. To fully demonstrate what can happen in a dual-

band push-pull amplifier that doesn't properly terminate the common-mode this section will show an ideal balun that is perfectly non-ideal at one of the common mode frequencies and go over the changes that occur with the drain currents and voltages. First to get a frame of reference we need to look at an ideal transformer. It's already been established thoroughly that baluns can be used to change a balanced signal, with equal currents in opposite directions into an unbalanced, or single-ended signal. Looking back at Fig. III-9 it is shown that the common mode voltage has many components inside it, instead of using an ideal transformer with infinite common mode impedance we'll instead use a transformer that has high impedance everywhere except at one of these intermodulation terms, for this example, 2 GHz. This will have the effect of changing the current flowing through the common-mode port, and if we apply the ideal balun formulas for the circuit shown in Fig III-7, we can calculate the new balanced currents.

Earlier, the common-mode current was never calculated beyond its DC component because it didn't make any sense too. The ideal choke simply terminates all frequencies with an infinite impedance, so of course the common mode current is equal to zero. However, now that the balun has low common mode impedance at an intermodulation term, the common mode current will have an AC component at exactly 2GHz. That common-mode term we can use to recalculate the drain currents by rearranging the terms in (III-17) and (III-18). Then the drain currents can be solved for independently and it can be seen how the common mode current has affected it.

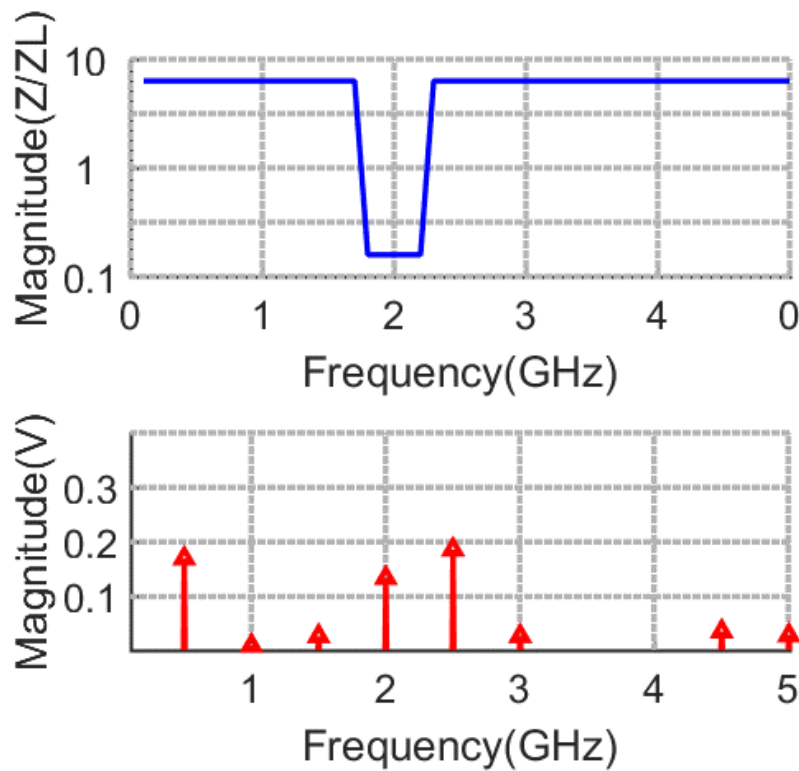


Figure III-12 Precisely non-ideal balun that has low common mode impedance at exactly 2 GHz

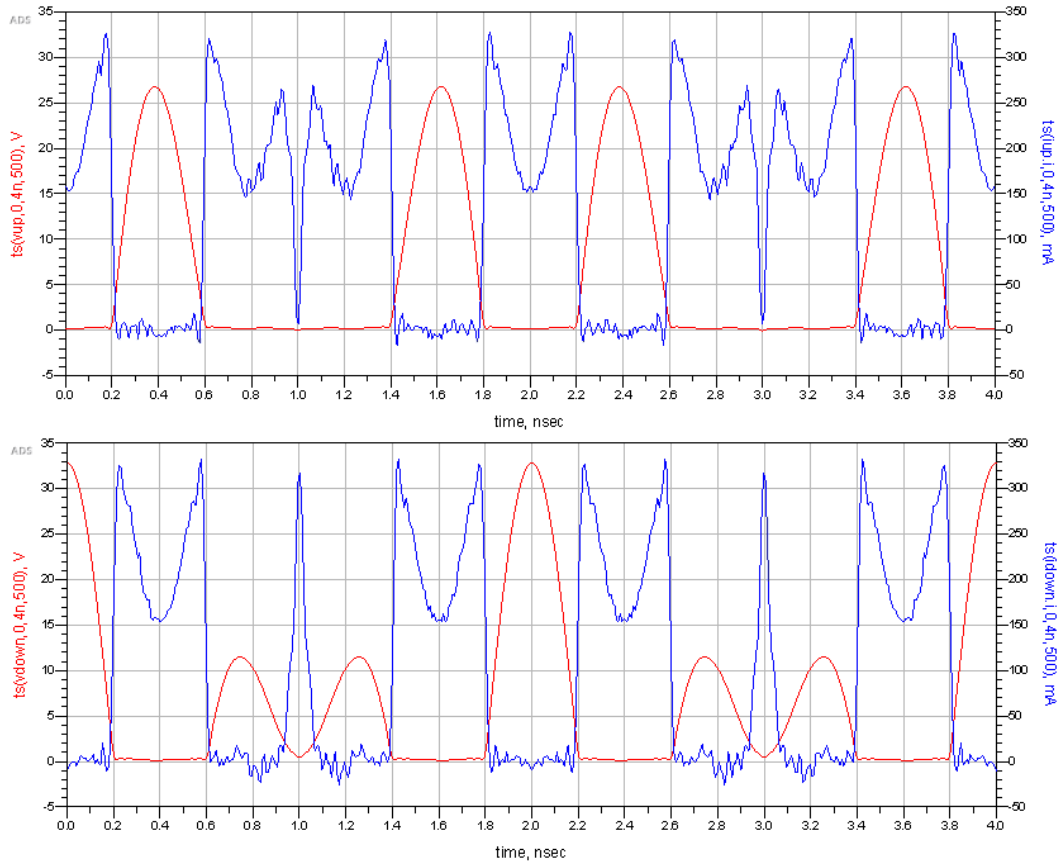


Figure III-13 New drain currents and voltages using a non-ideal balun

The distortion introduced to the drain currents has reduced the power in the pulse train that would have been filtered to find the fundamentals. That power that would have been headed towards the load is now consumed by the transformer which reduces the efficiency. The drain efficiency for the ideal class-D amplifier with this new perfectly non-ideal balun returns a drain efficiency of 81.6% giving us a loss of 11.4% which matches what table 1 predicts.

Now that it has been established that the common-mode voltage in dual band amplifiers can cause efficiency problems, this paper will now go over why a simple dual-band balun is not sufficient for solving them.

CHAPTER IV

DUAL-BAND BALUN DESIGN

4.1 Overview

This chapter will go over the basic methods involved in designing a balun for use in any dual-band system that does not have the new common-mode impedance requirements shown in the previous chapter. Systems such as those that prevent this efficiency loss from the common-mode do exist, but they have never been designed intentionally. Mostly the systems that can prevent this are ones with very broad common-mode impedance attributes, but they've not been used to combat this problem [12, 13, 14]. Other systems that are capable of preventing this are designed to specifically filter exact frequencies within the common-mode, but once again, the problems they were designed to address are different than the ones shown in Chapter III [32]. First a pair of standard baluns for use in any push-pull system will be designed.

Something important to note, these baluns will appear to be desirable but they will not work in a concurrent-band, push-pull amplifier, after they have been designed, a methodology to alter the balun will be shown. As was mentioned in the introduction, there are three key parameters for balun designs, CMRR, insertion loss, and phase balance. CMRR is a measure of how well the balun rejects common mode signals that enter the differential port. These parameters do not give any information on what impedance is shown to these signals. This normally isn't an important distinction but different baluns utilize different effects for providing these three parameters. For example, rat-race couplers, an example of which is shown in Fig IV-

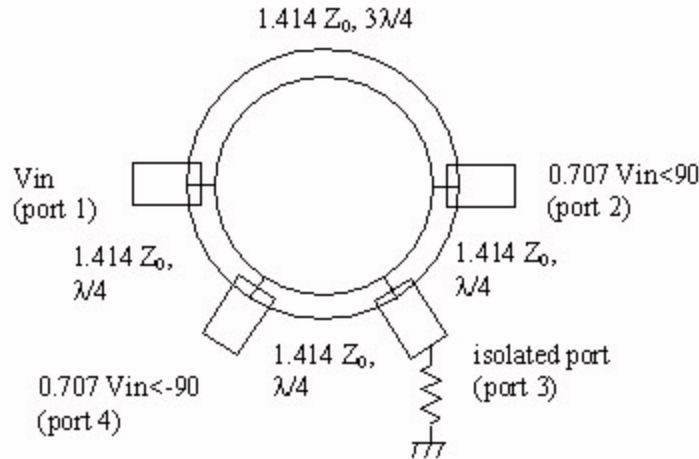


Figure IV-14 Example schematic for an ideal rat race coupler

15 can be used as a balun as well, but the method they use for common-mode rejection doesn't give the characteristics needed. There is an isolated port present in these designs that is terminated in 50 ohms, and the two differential ports are varying wavelengths of distance away such that any signals that are equal in phase and frequency cancel out. This is not necessarily desirable, because the common mode signals meet at the isolated port that means currents are still flowing and can still be distorting your drain currents.

Marchand baluns are among the simplest and most popular balun structures to design, due to their wide operating range and ease of implementation [21]. Marchand originally designed his balun using two coaxial transmission lines, each a quarter wavelength long at the design frequency [20, 23]. The shields of each coax were used for the differential signals respectively, while the center conductor was used for the single ended output. Since then, several papers have been published changing these coaxial baluns to their planar forms [22]. Their ease of design is one of the reasons coaxial transmission line baluns and transformers have been so common, they provide significant performance benefits over their planar cousins while being easier to design. As was stated earlier, designers working in the gigahertz ranges who want to take advantage of

differential signaling don't want to also have to fit a pair of coaxial transmission lines or a large transformer onto their boards. Many designers have come up with ways to convert Marchand's designs to their planar forms simply for the reduction in physical dimensions. Regardless of whether the balun is planar, coaxial, or ferrite based, in single-band or wide-band baluns the quarter-wavelength frequency of the balun will be a common-mode open and a differential-mode match, the common-mode open will rotate around the outside edge of the Smith chart as the signal moves farther away from the quarter-wavelength frequency, leaving many other frequencies close to a short. To demonstrate this, the next section will go over the design of some popular balun designs, step-by-step.

4.2 Planar Coupled Line Marchand Balun

The planar form of the Marchand balun has gone through several iterations of development, its current most popular form consists of two sets of coupled lines. The coupled line sections are each a quarter wavelength long, the balanced end of the balun is terminated to ground, while the single-ended side is terminated with the load at one end and an open or short on the other end [18].

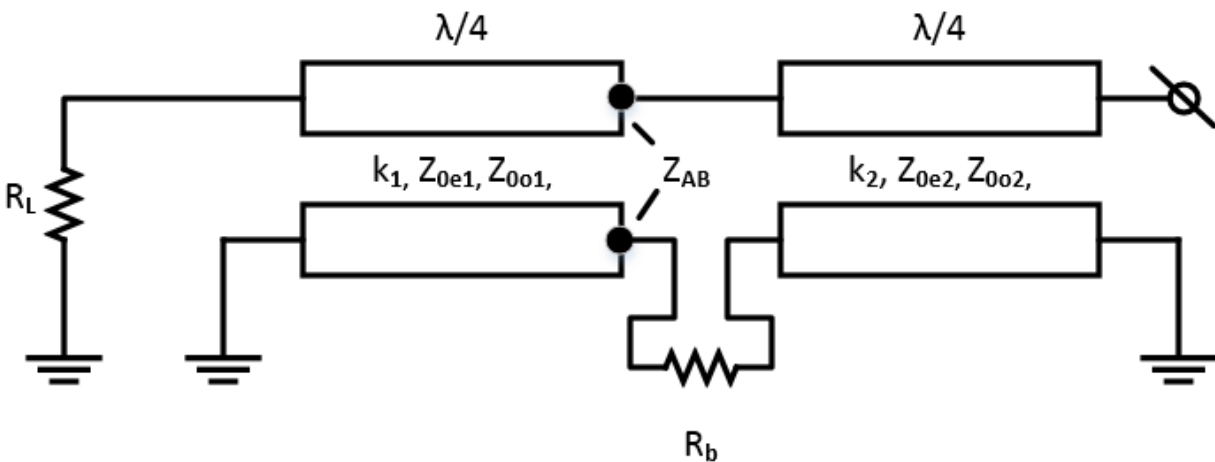


Figure IV-15 Example schematic for planar Marchand balun.

The flexibility of this structure is one of its advantages, many researchers have developed numerous ways to configure these baluns to fit nearly any frequency and impedance [21, 24]. To begin the design of this balun you first need to determine the physical quarter wavelength of the center frequency, almost all the other parameters of this balun are governed by the limits of your manufacturing process. The characteristic impedance of the coupled lines is used to generate the physical dimensions needed.

$$Z_{0x} = \sqrt{Z_{0ex}Z_{0ox}} = \frac{1}{Y_0}, k_x = \frac{Z_{0ex} - Z_{0ox}}{Z_{0ex} + Z_{0ox}} \quad (\text{IV-26})$$

Marchand showed in his design that the impedance between the coupled line sections but before the balanced load is equal to

$$Z_{AB} = \frac{jZ_b Z_{0s} \tan(\theta)}{Z_b + jZ_{02} \tan(\theta)} - jZ_{02} \cot(\theta) \quad (\text{IV-27})$$

And when the coupled line stub is at resonance $Z_{AB} = Z_b$, for a matched condition. Marchand also showed that for a wider bandwidth response the stubbed section of coupled lines should have a large characteristic impedance. Next, Z_{AB} needs to be matched to the input of the circuit or

$$Z_L = \frac{Z_{01}^2}{Z_b} \quad (\text{IV-28})$$

Using the first set of coupled lines we can set

$$Z_{0o1} = \frac{1}{2} \sqrt{Z_L Z_b} \quad (\text{IV-29})$$

Thus the only two things that need to be set are the odd mode of the first set, and the high even mode impedance of the second set. The parameters limiting the design now are the limits of your manufacturing process, once you've set Z_{01} and Z_{02} the physical dimensions can be found using the coupled line equations or a simpler method is to use Keysight's Linecalc or Hyperlynx's

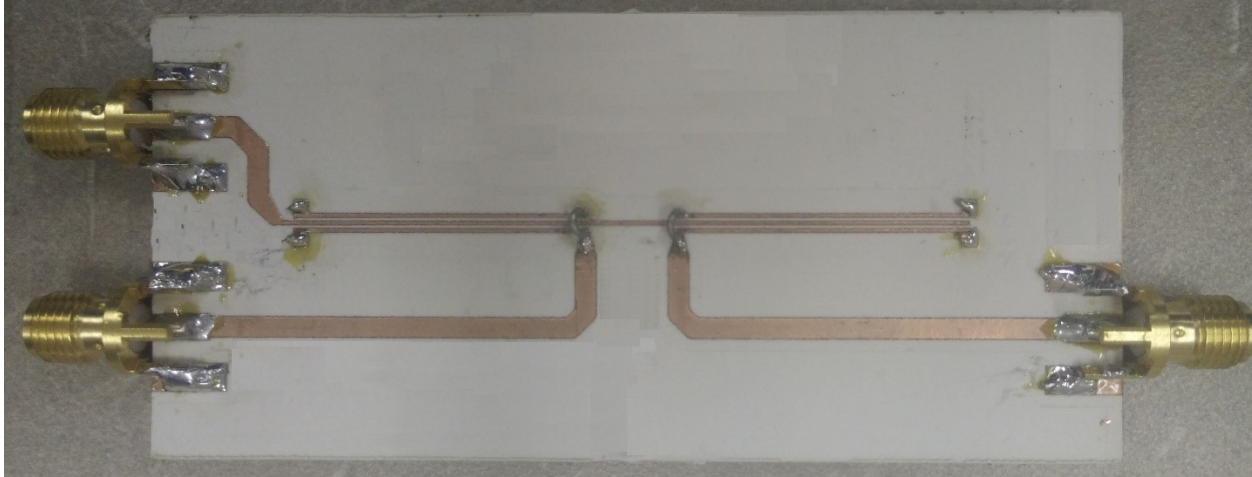


Figure IV-16 *Fabricated Marchand balun on RO3003 material.*

differential line utility. The balun designed here uses an additional coupled line that helps to increase the coupling factor through the added capacitance from the additional parallel surface area, thereby improving the CMRR [27]. Continuing with the frequencies chosen for the amplifier earlier of 1 GHz and 1.5 GHz fundamental frequencies, this balun is able to pass both the fundamentals while providing high CMRR at a wide bandwidth around the center frequency.

The final dimensions of the balun shown in Fig IV-16 are as follows; both the inner and outer conductors of each set of coupled line are 15 mils wide, with 980 mils in length on the active coupled lines, and 1000 mils length for the balancing stub. The spaces separating the conductors are approximately equal to 8 mils wide. The segment connecting the center conductor between the two coupled lines is 125 mils in length. It was fabricated on Rogers RO3003 with 30 mil thick board material, and 1oz copper weight. The reader will notice there is a set of long transmission lines running to the balanced input of the balun in Fig. IV-17 those were used to adjust the common mode impedance which will be discussed later. After being fabricated the s-parameters for this device were taken on a 4-port network analyzer and then used in Keysight's ADS to extract the resulting even and odd mode S-parameters.

The resulting insertion loss for the balun is shown in Fig. IV-18, the simulation results and measurement results are within 0.5 dB of each other at the two fundamental frequencies and also shows a CMRR of 15 dB or greater at the two fundamental frequencies. But as was previously discussed, these two parameters do not provide sufficient information to determine if it can be used in a dual-band switched-mode amplifier. The test setup for performing this measurement is given in Appendix C.

In order for this balun to be useful in a dual-band push-pull amplifier it needs to have high common-mode impedance at all of the intermodulation frequencies to maintain high efficiency. The common mode impedance has been plotted in Fig. IV-19 and it shows a sharp notch directly centered at 2 GHz as well as low impedance at 500 MHz, back in Chapter III it

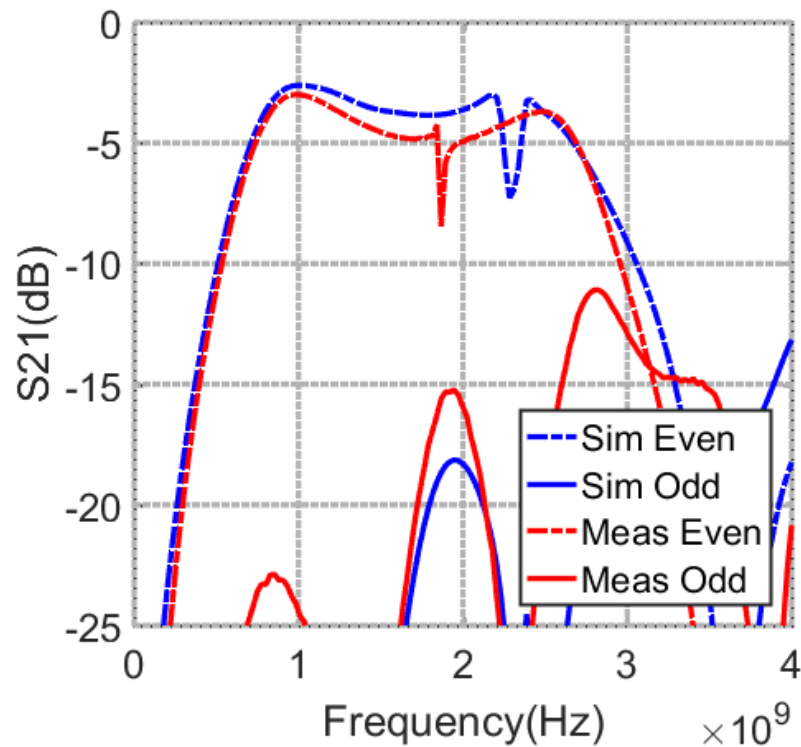


Figure IV-17 *S21 for both even and odd mode excitations from the balanced input to the single ended output*

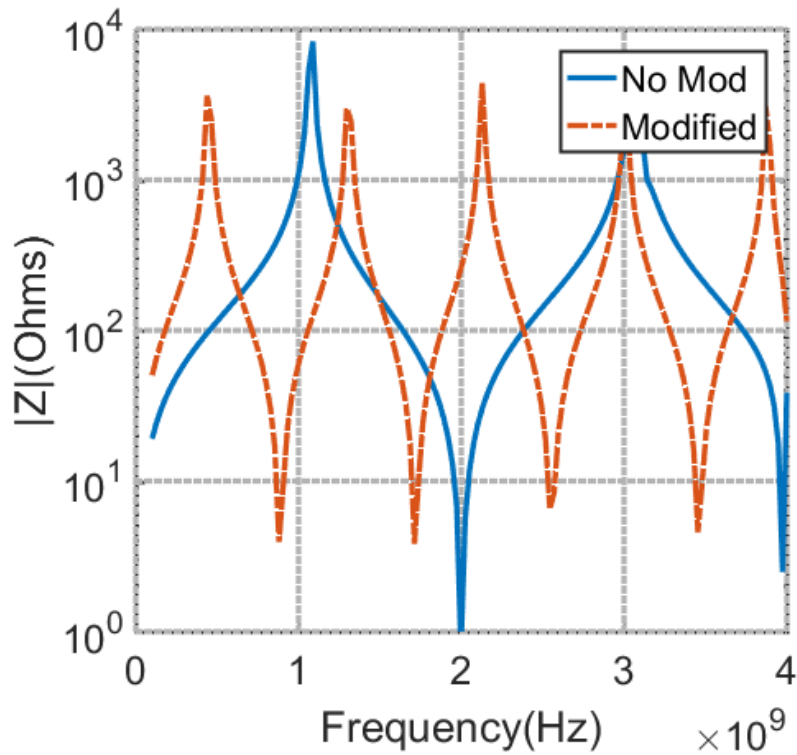


Figure IV-18 Magnitude of the common-mode impedance for the fabricated planar Marchand balun

was explained that both even harmonics and intermodulation components need to see high common-mode impedance. Testing this balun now with a class-D amplifier returns an efficiency of 53%.

In order to get some of that efficiency back, modifications will need to be made to this balun. To reiterate, Fig. IV-19 shows the magnitude of the common mode impedance for the balun before as well as after modifications were made. Without modifications, it shows that the impedance at both 2 GHz and .500 MHz is fairly low, low enough to waste significant efficiency when simulated with an ideal class-D amplifier. Since it's known that baluns use quarter wavelength effects to generate the desired common-mode rejection and power splitting,

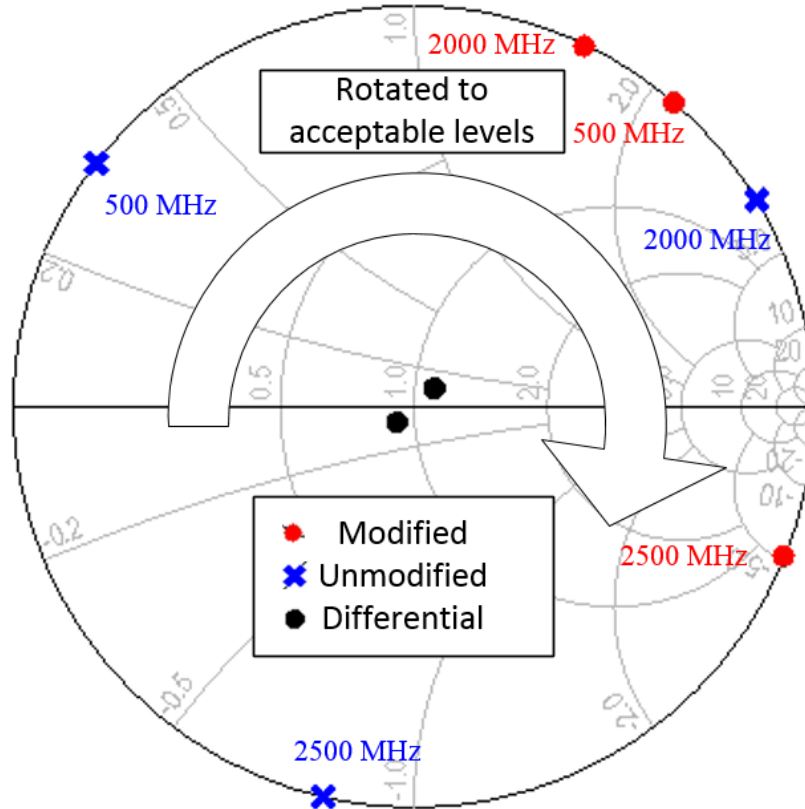


Figure IV-19 Rotation of the common-mode frequencies to higher magnitude impedance for the fabricated Marchand balun

transmission lines can be added to the front of the balanced port. These transmission lines will rotate the common mode impedance seen at the balanced port which is shown in Fig. IV-20.

Simply align the peaks with corresponding intermodulation components so that efficiency is not wasted. The end result of the modified balun when used in conjunction with an ideal class-D amplifier is a drain efficiency of 80.5% giving a total efficiency savings of 27.5% just by rotating the common mode impedance. The results of this exercise is recorded into Table II and agrees with the overall conclusions of Chapter III, that high-common mode impedance at intermodulation frequencies will save efficiency.

TABLE II. Ideal Class-D Efficiency with Marchand Balun

Balun	Efficiency
Ideal	93.0%
Without Modifications	53.0%
With Modifications.	80.5%

To demonstrate that this method can be used with other balun varieties, this paper will now move into the design of a different balun.

4.3 Multisection Coupled Line Marchand Balun

Multisection coupled line baluns are another simple variety of balun that utilizes coupled lines and quarter-wave effects to achieve the desired power splitting and phase balancing effects baluns are used for. The significant benefit of this structure is its repeating nature, it can be cascaded indefinitely assuming the designer has adequate space, in fact the more sections that are used in one of these baluns, the better their performance becomes [22, 25]. The limiting factor in these designs is size, since each section is a quarter-wavelength long in the lower GHz ranges these become quite long and unwieldy.

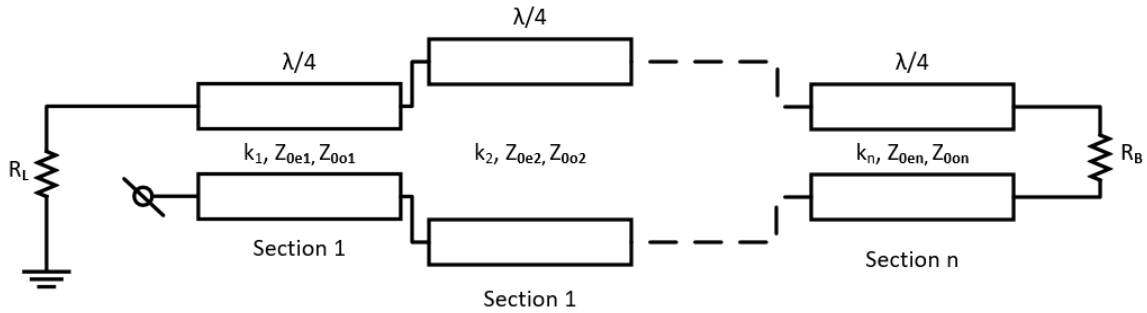


Figure IV-20 Example schematic for a multisection coupled line balun.

Like the planar Marchand balun, very high common-mode impedance is required for adequate performance, and by cascading many different coupled line structures Z_{0e} can be made as high as needed. This allows designers to utilize simple two-layer designs instead of using embedded microstrip lines, or coaxial segments, just by cascading more structures. Figure IV-21 shows an example schematic for a multisection coupled line balun where n is the number of coupled line sections in the balun. Starting from the single-ended section the coupled line sections are set in series and one terminal ends with an open circuit or short circuit. The odd mode impedances multiply together to get the effective Z_{0o} , the same is true for the even mode. If we go back to equation IV-30, which is the formula for the impedances of a single pair of coupled lines. It's shown that coupled lines possess both even and odd mode impedances and if we take the even and odd mode equivalent circuits of a sequence of coupled lines it converts down to just a series of different transmission lines with Z_{0e} or Z_{0o} as characteristic impedances. Since it's known that a series of transmission lines with a differing impedance can be treated as a single transmission line with an effective impedance [26], the same can be done with the equivalent circuits. The effective impedance of the cascade of coupled lines is given as follows:

When n is odd;

$$Z_{0o} = \frac{Z_{0o1} * Z_{0o3} * \dots * Z_{0on}}{Z_{0o2} * Z_{0o4} * \dots * Z_{0o(n-1)}} \quad (IV-30)$$

$$Z_{0e} = \frac{Z_{0e1} * Z_{0e3} * \dots * Z_{0en}}{Z_{0e2} * Z_{0e4} * \dots * Z_{0e(n-1)}} \quad (IV-31)$$

When n is even;

$$Z_{0o} = \frac{Z_{0o1} * Z_{0o3} * \dots * Z_{0o(n-1)} * Z_{out}}{Z_{0o2} * Z_{0o4} * \dots * Z_{0on}} \quad (IV-32)$$

$$Z_{0e} = \frac{Z_{0e1} * Z_{0e3} * \dots * Z_{0e(n-1)} * Z_{out}}{Z_{0e2} * Z_{0e4} * \dots * Z_{0en}} \quad (IV-33)$$

This balun was also designed to work at both 1GHz and 1.5GHz and built on Rogers RO3003. The dimensions for its construction are given here. The tightly coupled sections have linewidths of 13.6 mils with the space between them equal to 8.6 mils. The loosely coupled sections have 36 mil linewidths, and 160 mils of space between them. After being fabricated, the s-parameters for this device were recorded using a 4-port network analyzer, once the data was taken it was placed inside ADS and simulated with common mode excitations to extract the s-parameter data shown in Fig. IV-21.

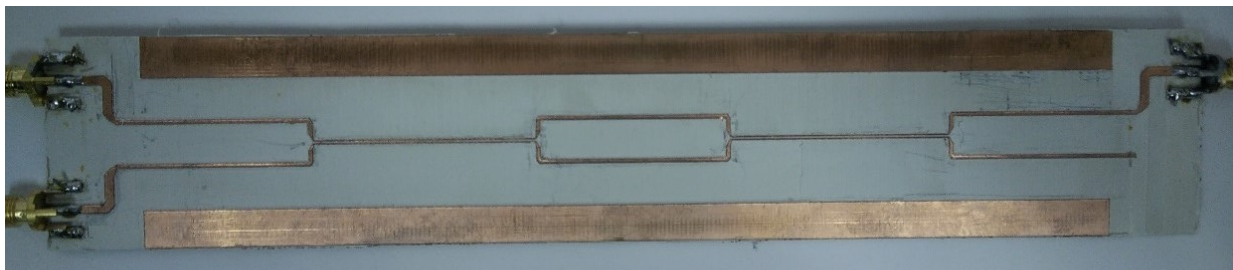


Figure IV-22 Fabricated multisection coupled line balun.

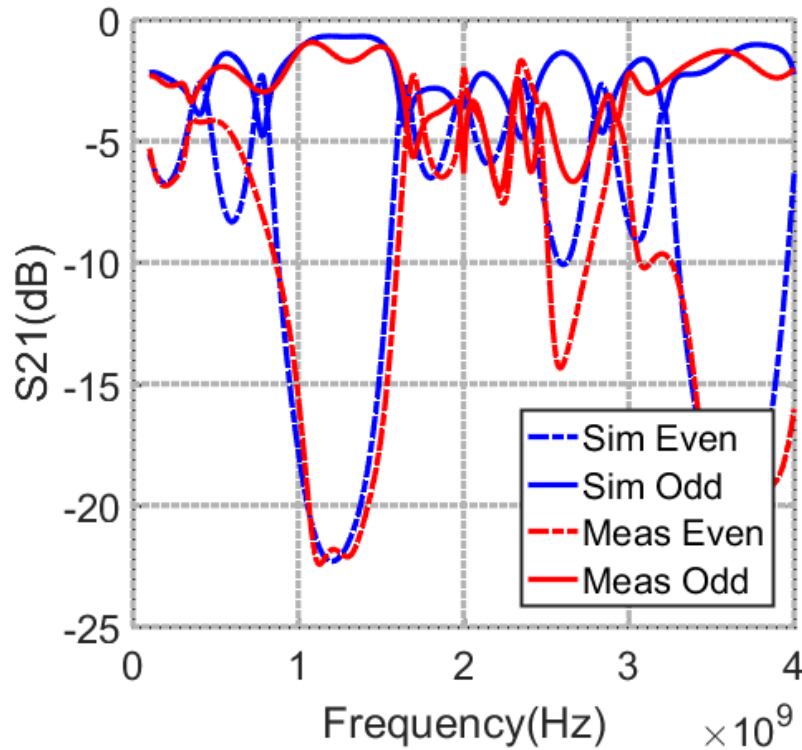


Figure IV-23 S_{21} for both the manufactured and simulated forms of the multisecton coupled line balun.

At both of the fundamental frequencies there is less than .3dB of difference between simulated and measured insertion loss. Also of note is that there is at least 15 dB of CMRR, this seems low but there are only two tightly coupled sections in this balun, using more would result in higher CMRR. Regardless, as was mentioned earlier, this balun has already been designed and used in dual-band systems, but never used in a dual-band push-pull amplifier. In order for it to be used in a dual band system the common mode impedance at the intermodulation frequencies must be examined.

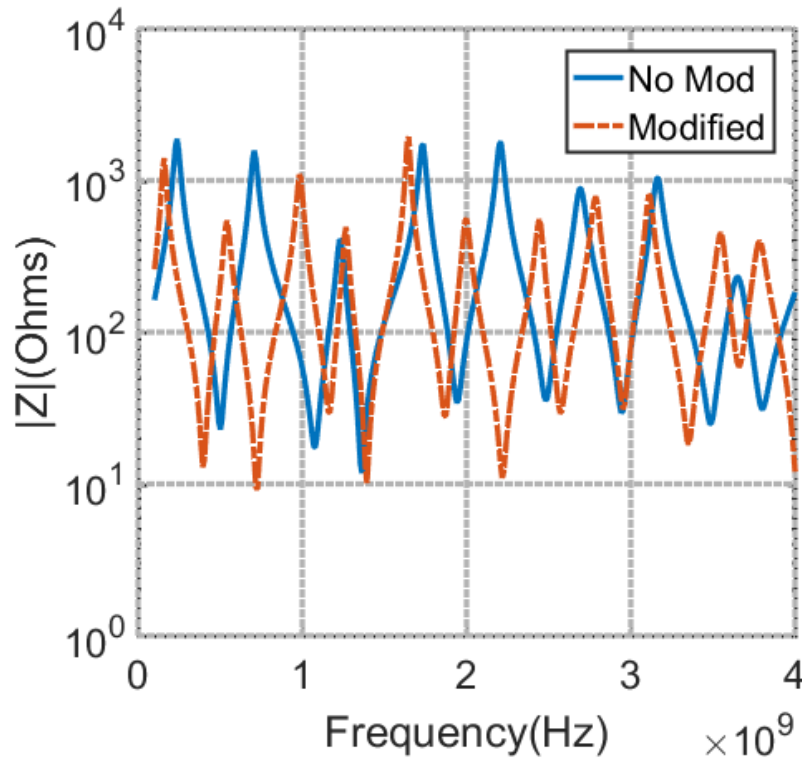


Figure IV-24 Magnitude of the common mode impedance before and after the set of balun transmission lines were added.

Figure IV-24 shows the magnitude of the common-mode impedance for the multisection coupled line balun, the most serious frequencies of note here are 500 MHz. Without any modifications there's a notch centered directly at 500 MHz, that by itself looking at the table generated earlier will waste nearly 10% overall efficiency. Another notch of note is 2.5 GHz, which corresponds to f_1+f_2 , again wasting almost 8% efficiency.

TABLE III. Ideal Class-D Efficiency with Multisection Coupled Line Balun

Balun	Efficiency
Ideal	93.0%
Without Modifications	49.1%
With Modifications.	72.1%

Table 3 summarizes the resulting efficiency when using the measured s-parameters from the multisection coupled line balun alongside an ideal push-pull class-D amplifier. This balun still provides some efficiency benefit, but it wasn't as effective as the planar Marchand balun, mostly due to the lower common-mode impedances it provides as well as the poorer matching conditions. The sheer number of intermodulation components that all need to see high common-mode impedance make it very challenging to make a clear connection to efficiency loss due to this issue.

CHAPTER V

CONCLUSIONS AND FUTURE WORK

5.1 Conclusion

This thesis has gone over the maximum theoretical efficiency for push-pull class-D power amplifiers and expanded it using sources to the dual-band case. Then using MATLAB calculations and ADS simulations verified the maximum efficiency of a dual-band push-pull class-D power amplifier. Once that had been established this paper looked the currents and voltages at the common node of an ideal transformer and saw that there were indeed many more components in the common-mode voltage than in the single band case. These intermodulation components were explored further and go on to explain why some designers would see efficiency losses if they attempted to use a balun that didn't terminate these common-mode intermodulation components with an open. This paper then performed a simulation on using an ideally non-ideal balun in place of a perfectly ideal one to see exactly how the mechanics behind this efficiency loss work. With the Drain currents becoming more distorted as the intermodulation components see lower and lower impedance. Finally this thesis went over a method of modifying existing baluns with a simple addition of transmission lines to add common-mode impedance where needed and verified that this did indeed save the approximate amount of efficiency as predicted. This shows that the CMRR of a balun isn't as important as the common-mode impedance when dealing with dual-band push-pull amplifiers.

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APPENDIX A

MATLAB SCRIPT FOR CLASS-D EFFICIENCY

```

clear all
close all
%IDEAL BALUN
%vdiff = vplus - vminus;
%vcom = (vplus + vminus)/2;
%idiff = -1*(iplus - iminus)/2;
%icom = -1*(iplus + iminus);
Fs = 100e9; %Sampling Freq
L = 16384; %#of samples
Ts = 1/Fs; %Length of Signal
t = (0:L-1).*Ts; %Time vector
NFFT = 2^nextpow2(L); %for FFT
xx = 800;
%generate input voltage waveforms
F1 = 1e9; F2 = 1.5e9;
T1 = F1^-1; T2 = F2^-1;
w1 = F1*2*pi; w2 = F2*2*pi;
phi = 0; %phi = 4/5*pi;
rl = 1; %load
vinup = cos(w1*t) + cos(w2*(t+phi));
vindow = -1*(cos(w1*t) + cos(w2*(t+phi)));
%generate drain currents from input
iup = zeros(1,L);
idown = zeros(1,L);
for i = 1:L
    if vinup(i) > 0
        iup(i) = 1;
    else
        iup(i) = 0;
    end
    if vindow(i) > 0
        idown(i) = 1;
    else
        idown(i) = 0;
    end
end
%generate balun currents
idiff = -1.*(iup - idown)./2;
icom = -1.*(iup + idown);
Id = fft(idiff,NFFT)/L;
ff = Fs/2*linspace(0,1,NFFT/2+1);
window = .05e9;
fli = find(ff > F1-window & ff < F1+window);
f2i = find(ff > F2-window & ff < F2+window);
% figure(6);
% subplot(211);
% plot(t,iup,t,idown,'red');
% title('initial drain currents');
% axis([0,4e-9,-.2,1.2])
% subplot(212);
% plot(ff,2*abs(Id(1:NFFT/2+1)));
% xlim([0 10e9])

```

```

figure; subplot(211);
plot(t(1:xx),idiff(1:xx));
title('ideal differential current');
subplot(212);
plot(ff,2*abs(Id(1:NFFT/2+1)));
xlim([0 10e9])
%brick wall filter out all but fundamental;
scan_Id = 2*abs(Id(1:NFFT/2+1));
a1 = max(scan_Id(min(f1i):max(f1i)));
f1 = find(scan_Id == a1);
f1 = ff(f1);
a2 = max(scan_Id(min(f2i):max(f2i)));
f2 = find(scan_Id == a2);
f2 = ff(f2);
ifund = a1*cos(2*pi*f1*(t)) + a2*cos(2*pi*f2*(t+phi));
vdiff = ifund*rl;
figure; hold on;
title('differential voltage');
plot(t(1:xx),vdiff(1:xx)); hold off;
%generate drain voltages
vrect = abs(vdiff);
vup = (abs(-1.*(iup)+1).*vrect);
vdown = (abs(-1.*(idown)+1).*vrect);
figure(); subplot(211); hold on;
title('drain voltage and current');
plot(t(1:xx),vup(1:xx),'red');
plot(t(1:xx),iup(1:xx),'blue');
hold off;
subplot(212); hold on;
plot(t(1:xx),vdown(1:xx),'red');
plot(t(1:xx),idown(1:xx),'blue');
hold off;
%find common mode voltage
vcom = (vup + vdown)/2;
Vcom = fft(vcom,NFFT)/L;
figure; subplot(211);
plot(t(1:xx/2),vcom(1:xx/2));
title('common mode voltage');
subplot(212);
plot(ff,2*abs(Vcom(1:NFFT/2+1)));
xlim([100e6 6e9]);
%ideal efficiency
vdc = abs(mean(vcom));
idc = abs(mean(icom));
pdc = idc*vdc;
pout = (rms(ifund)^2)*rl;
n = pout/pdc;
%manually reconstruct IM components out of the common mode voltage;
scan_Vcom = 2*abs(Vcom(1:NFFT/2+1));
scan_Vcom(1:50) = 0;
scanned = 15;
%freq, amp
im(1:6,1:2) = 0;
[im(1,2), im(1,1)] = max(scan_Vcom);
scan_Vcom(im(1,1)-scanned:im(1,1)+scanned) = 0;
im(1,1) = ff(im(1,1));
[im(2,2), im(2,1)] = max(scan_Vcom);

```

```

scan_Vcom(im(2,1)-scanned:im(2,1)+scanned) = 0;
im(2,1) = ff(im(2,1));
[im(3,2), im(3,1)] = max(scan_Vcom);
scan_Vcom(im(3,1)-scanned:im(3,1)+scanned) = 0;
im(3,1) = ff(im(3,1));
[im(4,2), im(4,1)] = max(scan_Vcom);
scan_Vcom(im(4,1)-scanned:im(4,1)+scanned) = 0;
im(4,1) = ff(im(4,1));
[im(5,2), im(5,1)] = max(scan_Vcom);
scan_Vcom(im(5,1)-scanned:im(5,1)+scanned) = 0;
im(5,1) = ff(im(5,1));
[im(6,2), im(6,1)] = max(scan_Vcom);
scan_Vcom(im(6,1)-scanned:im(6,1)+scanned) = 0;
im(6,1) = ff(im(6,1));
im = sortrows(im);
vcms(1:6,1:L) = 0;
vcms(1,1:L) = im(1,2)*cos(t*2*pi*im(1,1));
vcms(2,1:L) = im(2,2)*cos(t*2*pi*im(2,1));
vcms(3,1:L) = im(3,2)*cos(t*2*pi*im(3,1));
vcms(4,1:L) = im(4,2)*cos(t*2*pi*im(4,1));
vcms(5,1:L) = im(5,2)*cos(t*2*pi*im(5,1));
vcms(6,1:L) = im(6,2)*cos(t*2*pi*im(6,1));
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%Set common mode impedance.
rc = [.1*rl .2*rl .5*rl rl rl*2 rl*5 rl*10 rl*1000];
for i = 1:8
    for j = 1:6
        %recalculate icom
        icomx = vcms(j,1:L)/rc(i);
        %recalculate drain currents
        iup2 = (iup - icomx).*iup;
        idown2 = (idown - icomx).*idown;
        %regenerate balun currents
        idiff2 = -1.*(iup2 - idown2)./2;
        icom2 = -1.*(iup2 + idown2);
        Id2 = fft(idiff2,NFFT)/L;
        %recalculate ifund and vdiff
        scan_Id2 = 2*abs(Id2(1:NFFT/2+1));
        a12 = max(scan_Id2(min(f1i):max(f1i)));
        f12 = find(scan_Id2 == a12);
        f12 = ff(f12);
        a22 = max(scan_Id2(min(f2i):max(f2i)));
        f22 = find(scan_Id2 == a22);
        f22 = ff(f22);
        ifund2 = a12*cos(2*pi*f12*(t)) + a22*cos(2*pi*f22*(t+phi));
        vdiff2 = ifund2*rl;
        %regenerate drain voltages
        vrect = abs(vdiff2);
        vup2 = (abs(-1.*(iup)+1)).*vrect);
        vdown2 = (abs(-1.*(idown)+1)).*vrect);
        %find common mode voltage
        vcom2 = (vup2 + vdown2)/2;
        Vcom2 = fft(vcom2,NFFT)/L;
        %non-ideal efficiency
        vdc2 = abs(mean(vcom2));
        idc2 = abs(mean(icom2)) + rms(icomx);
        pdc2 = idc2*vdc2;
    end
end

```

```

pout2 = (rms(ifund2)^2)*rl;
n2(i,j,1) = pout2/pdc2;
if i == 1 && j == 3
    figure;
    plot(t(1:xx),icomx(1:xx));
    title('non-ideal common mode current');
    figure; subplot(211); hold on;
    title('non-ideal drain voltage and current');
    plot(t(1:xx),vup2(1:xx),'red');
    plot(t(1:xx),iup2(1:xx),'blue');
    hold off; subplot(212); hold on;
    plot(t(1:xx),vdown2(1:xx),'red');
    plot(t(1:xx),idown2(1:xx),'blue');
    hold off; figure; subplot(211);
    plot(t(1:xx),idiff2(1:xx));
    title('non-ideal differential current');
    subplot(212);
    plot(ff,2*abs(Id2(1:NFFT/2+1)));
    xlim([0 10e9])
end
end
end

n2(8,1) - n2

```

APPENDIX B

FOURIER SERIES FOR RECTIFIED SUM OF SINES

$$\left\{ \begin{array}{ll} 0 & \text{if } \sigma_1 = 0 \\ \sigma_2 & \text{if } 0 < \sigma_1 \\ -\sigma_2 & \text{if } \sigma_1 < 0 \\ \int e^{t w} |\sigma_1| dw & \text{if } -\sigma_1 < 0 \wedge -0 \leq \sigma_1 \end{array} \right.$$

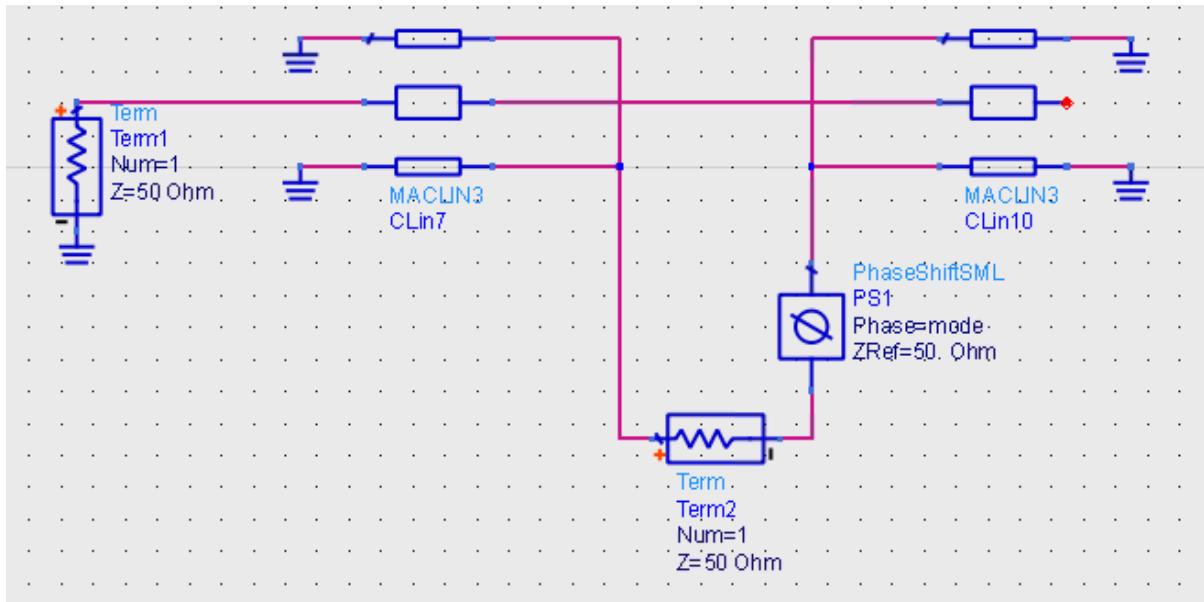
where

$$\sigma_1 = \sin(t w x) + \sin(t w)$$

$$\sigma_2 = \frac{e^{t w} (2 \sin(t w x) - \cos(t w) + \sin(t w) - x^2 \cos(t w) + x^2 \sin(t w) - 2 x \cos(t w x))}{2 t (x^2 + 1)}$$

APPENDIX C

ADS TEST SETUP FOR EVEN-ODD MODE S-PARAMETERS



All even-odd mode measurements were taken using this setup, the differential S21 can be found by setting the Phase variable of the PhaseShifter block to 180, and the even mode, by setting Phase to 0.